Proposal for extended closeout activity for pixel R&D

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Jim Strait's charge for this meeting

"I'd like to hear from you and your colleagues about the following:

- A summary of what has been accomplished so far on the BTeV pixels.
- A statement of the goals of the proposed R&D program.
- A description of the work you propose to do, including a clear definition of what constitutes completion of the R&D.

Jim’s charge

- A description of what will be learned from the R&D and how that can benefit future experiments. The more specific you can be about demonstrating the interest of others in the results the better.
- An estimate of the expected M&S costs.
- An estimate of the labor needed, including scientific as well as other technical labor, in PPD and in other Divisions. The more specific you can be about specific people who will be involved the better.

Jim’s charge

- A summary of the demands this will place on the lab's facilities, e.g. the test beam, SiDet, etc.
- A schedule estimate.
- A summary of the risks, e.g. the risk that the work will take substantially longer or cost substantially more than you estimate, or the risk that you do not accomplish your R&D goals.”

Outline of this presentation

- Context of Fermilab pixel R&D (BTeV).
- Advantages of hybrid silicon pixels.
- Responses to each of Jim's 9 topics.
- Summary.

Context

- BTeV was possible because of two "enabling technologies."
  1. A silicon pixel detector with very high segmentation and very fast, zero suppressed, readout.
  2. A vertex trigger (using pixel hits) capable of accepting data from more than 15 million events per second, selecting events containing measurable b decays, and rejecting backgrounds.

Context

- However, it was also recognized that silicon pixel detectors were likely to be valuable for other experiments besides BTeV.
  - From 1997 to 2004, pixel R&D was funded separately from BTeV (through the “radiation hard vertex detector” group in EPP).
  - Pixel R&D was subsumed by BTeV in FY2004 in recognition of the fact that *most* of the remaining development effort was “BTeV-specific.”
    - Operation in the Tevatron machine vacuum.
    - Need to move away from the beam before each store, and then back to within 6mm of the beamline after stable Collider operations had been established.

Advantages of hybrid silicon pixel detectors

- Pattern recognition power
  - 23 million channels in BTeV pixel detector → by far the lowest occupancy subdetector, even located 6mm from the colliding beams.
  - Spacepoints make pattern recognition "trivial."

Advantages of hybrid silicon pixel detectors

- Excellent spatial resolution
  - High stopping power of silicon:
    - Most ionization is contained within a few microns of a track.
    - A minimum ionizing particle creates 80 e/h pairs per micron of track length.
  - Low noise electronics:
    - Small sensor pixel and bump bonding means very small input capacitance.
    - Separate development of sensor and readout chip allows each to be optimized.

Advantages of hybrid silicon pixel detectors

- Radiation hardness
  - Sensor damage is primarily hadronic.
    - Hadrons displace silicon nuclei from the lattice; effectively increasing the p-dopant concentration.
    - N-type material becomes almost intrinsic (depletion voltage approaches zero), then “type inverts” and becomes increasingly p-type (depletion voltage increases with dose).
    - *N-in-n pixel detectors can be operated after type inversion at less than full depletion voltage; lower noise electronics (compared to silicon strip detectors) means efficient operation is possible even with reduced signal and increased noise (due to leakage current)*.

Advantages of hybrid silicon pixel detectors

- Radiation hardness
  - CMOS damage is primarily electromagnetic.
    - Glass insulating layer becomes positively charged (glass rod & rabbit's fur), resulting in "threshold shifts."
    - Explicitly radiation tolerant processes relied on secret chemistry to bleed off trapped charge.
    - In "deep submicron" CMOS processes, quantum tunneling removes trapped charge from thin "gate oxide."
      - "Enclosed geometry" transistor layout and guard rings solve problems caused by trapped charge in thicker "field oxide."

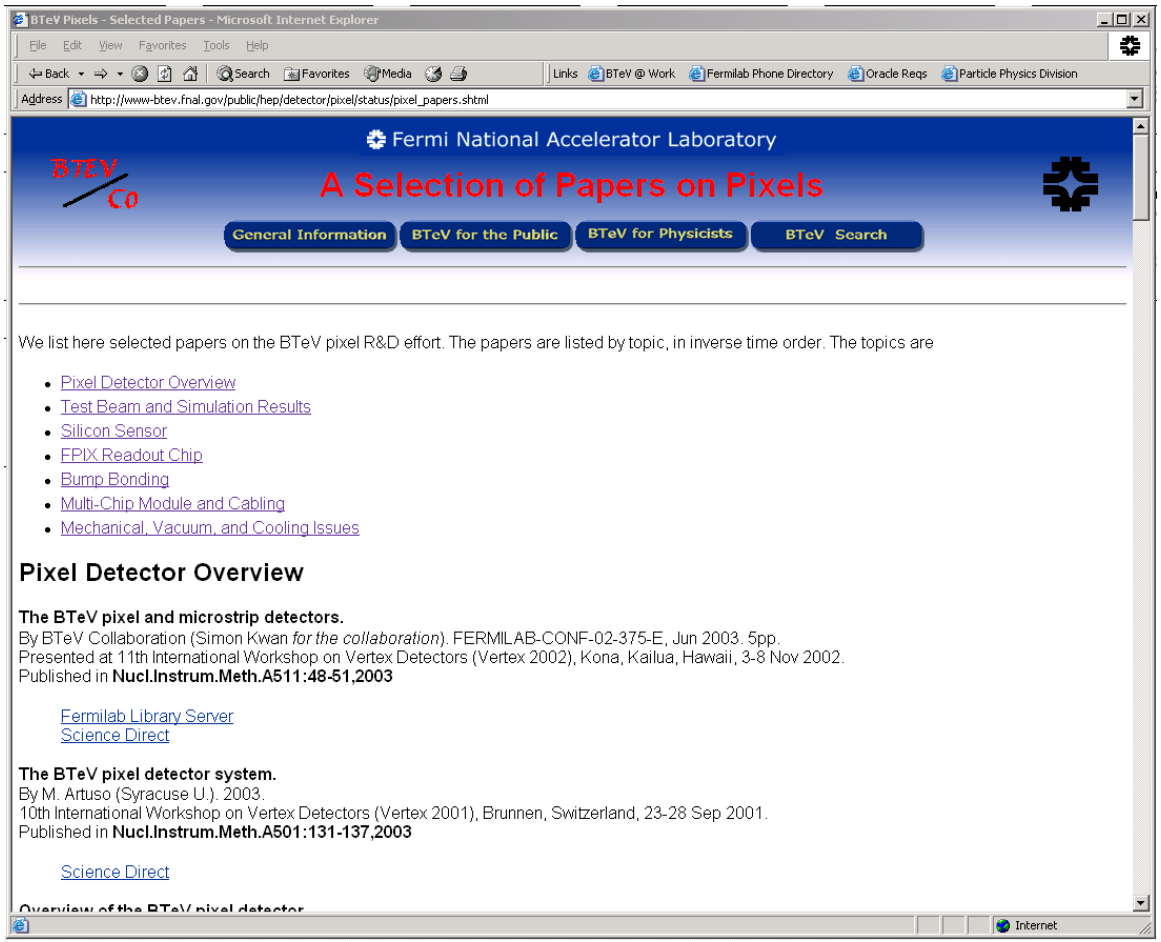
Pixel R&D Team

- **Iowa:** Divoky, Newsom, Morgan
- **Fermilab:** Andresen, Appel, Austin, Butler, Cancelo, Cardoso, Catalanello, Cease, Chiodini, Christian, Cihangir, Demaat, Deurling, Dychakowsky, Dyer, Fast, Franzen, Gingu, Grimm, Hall, Hoff, Howell, Jakubowski, Jones, Kendziora, Kozlovsky, Kutschke, Kwan, Larwill, Lei, Mateski, Marinelli, Mekkaoui, Moibenko, Montes, Pavlicek, Prosser, Rauch, Ruschman, Sanders, Sellberg, Shenai, Skup, Slimmer, Tope, Turqueti, Tweed, Uplegger, Wester, Yarema, Zhang
- **Frascati:** Bianco, Caponero, Colonna, Fabbri, Paolozzi
- **Milano:** Alimonti, Magni, Menasce, Moroni, Pedrini, Sala
- **New Mexico:** Papavassiliou
- **Syracuse:** Artuso, Boulahouache, Wang
- **Tennessee:** Berridge, Handler
- **Wayne State:** Cinabro, Schreiner
- **Wisconsin:** Sheaff

This has been a significant multiyear effort.

Topic 1: Accomplishments

http://www-btev.fnal.gov/public/hep/detector/pixel/status/pixel_papers.shtml



MUCH has been accomplished: This web page lists 49 published papers. Significant advances have been made recently, especially in mechanical, vacuum, & cooling systems.

Topic 1: Major milestones in module R&D

Readout Chip	Sensor	Bumps	Advances
FPIX0 – 1997 (64x16) 0.8μ CMOS	ATLAS ST-1 (p-stop & p-spray) CiS & Seiko	Indium (Boeing) 1998	<100 e^- noise σ < 9μ with 2-3 ADC bits
FPIX1 – 1999 (160x18) 0.5μ CMOS	BTeV/CMS proto (p-stop) Sintef	Indium (AIT) & Solder (MCNC) 2000 – 2001	Readout speed (Column-parallel architecture)
FPIX2 – 2002 (128x22) 0.25μ CMOS	BTeV proto (moderated p-spray) Tesla	Indium (AIT) & Solder (VTT) 2002 – 2004	Radiation Hard Higher speed (~30 ns/hit), ease of use (DAC's & I/O) multichip modules beam tested

Topics 2/3: This Proposal

- Goal:
  - To finish the development of state-of-the-art hybrid silicon pixel detector modules.
- Completion criteria:
  - Demonstrate stable operation after irradiation.

Topics 2/3: This Proposal

1. Finish modifications to the FPIX2 readout chip.
   - Two failures must be corrected:
     - Readout hangs when multiple pixels are hit in ~200ps interval as BCO number is incrementing (design change is done).
     - Amplifier oscillates after irradiation with large leakage current.
2. Fabricate a modest number of wafers of FPIX readout chips.
3. Fabricate hybrid pixel modules using existing moderated p-spray silicon pixel detectors (this entails solder bump deposition and flip chip assembly).
4. Bench test and beam test hybrid sensors, both before and after irradiation.

Topic 4: Applications and benefits

- At the end of this activity, we will have working hybrid pixel detectors. Applications include:
- Any Tevatron experiment requiring precision tracking and high rate readout (including beam monitoring instrumentation).
- RHIC upgrade: LANL group has submitted a proposal to use our pixel detectors in PHENIX.
  - Gerd Kunde has volunteered $50k for R&D in FY05 & is interested in collaborating on module testing in FY06.
- ILC detector:
  - Our detectors would work well with the expected time structure of the cold machine; none of the thinner alternatives is yet proven.

Topic 4: Applications and benefits

- High QE 5-20 keV x-ray detection with fast readout:
  - P902: pion mass measurement using x-rays from pionic atoms.
  - x-ray crystallography:
    - Potential break-through detector for use at bright light sources such as APS & LCLS.
- LHC upgrade:
  - Our high readout rate architecture could be modified to support triggered operation.

Topic 5: Estimated M&S Cost

- $200k for TSMC engineering run through MOSIS (FY05)
  - ($0 – $50k incremental if combined with TripT)
- $120k for bump bonding (FY05)
- $20k for new HDI (flex circuit) (FY06)
- $10k for new PTA (pc interface) (FY06)
- $10k for test pcb's ($2k in FY05; $8k in FY06)
- $10k for misc. lab & test beam eqp. (FY06)
- $0 for irradiation at IUCF (use existing credit) (FY06)
- $50k has been offered by LANL (FY05)
- Totals:
  - **FY05: $72k – $322k**
  - **FY06: $48k**

Topic 6: Estimated labor

- **PPD**
  - ASIC design/layout (Mekkaoui, Hoff): 6 weeks
  - Single chip test pcb layout (Dychakowsky): 2 weeks
  - Chip testing (Christian, Mekkaoui, Hoff): 3 weeks x ½ time
  - Bump bond procurement (Kwan): 4 weeks x ¼ time
  - ASIC wafer probing (Gingu): 3 weeks
  - Module probing (Cihangir): 4 months x ½ time
  - Module assembly (SiDet senior tech): 2 months
  - Wire bonding (SiDet): 1-6 weeks
  - Module testing (bench & beam) (Christian): 1 year x ¼ - ½ time

Labor Type	FY	FTE-years 05	06
ElectDraft(M/W)		0.04	
EngP		0.06	0.16
EE		0.3	
TC Tech (M)			0.25
Sci		0.05	0.4
Total		0.45	0.81

- **CD**
  - PTA development, pixel module testing (bench & beam) (Cardoso, Turqueti, Uplegger): 1 ½ years (Cardoso ½ time)
  - PTA firmware: (Deuerling): 2 months
  - HDI design/layout (Andresen): 3 months
  - pcb layout (CD senior tech): 2 months

Labor Type	FY	FTE-years 05	06
EE		0.91	1.5
Senior Tech (M)		0.16	0.24
Sci		0.5	1
Total		1.57	2.74

Topic 7: Demands on facilities

Minimal Impact

- SciDet: Wafer probing (Cihangir) & Module assembly
- MTest: 2-3 running periods in spring-fall, 2006
  - Would like to use the existing BTeV pixel hut & probably the existing pixel telescope.
- FCC3 – Bench test area required through FY2006.

Topic 8: Schedule

- ASIC design: 4/1/05 – 5/31/05 (submission on 5/31).
- Chips received: End of August, 05.
- Chips tested; sensor & ASIC wafers sent for bumping: mid-end of September, 05.
- New HDI design complete: December 1, 05.
- New HDI tested: mid January, 06.
- Bump bonded parts received: Feb 1, 06.
- Module bench tests start: mid Feb, 06.
- Beam test of unirradiated parts: Spring, 06.
- Bench & beam test of irradiated parts: Early summer, 06.
- Bench & beam test of heavily irradiated parts: Late summer-fall, 06.

Topic 9: Risks

1. New FPIX chip may fail before irradiation (very low likelihood).
   - New submission would be required – schedule & cost impact.
   - Stop work; reassess the project (fall, 05).
2. Bump bonding may have zero yield (very low likelihood).
   - New sensor submission would be required – schedule/cost.
   - Stop work; reassess the project (winter/spring 06).
3. New HDI could be defective (low likelihood).
   - Schedule/labor/cost impact (~2-3 months + cost of Andresen's time (CD) + $20k M&S for new HDI).
4. New PTA could fail (low likelihood).
   - Possible schedule/labor/cost impact (CD EE time + $10k?)
   - Fallback = use previous generation PTA/PMC
5. New FPIX chip may fail after irradiation (low likelihood).
   - New chip & sensor submissions would be required – high impact.
   - Stop work; reassess the project (fall, 06).

Summary: Principle advantages with respect to ATLAS/CMS/ALICE pixels

- Readout speed.
  - Individual chip readout bandwidth is 7x faster than CMS pixel readout; all chips read out in parallel so full system is *much* faster.
- Ease of use.
  - Standard LVDS I/O → No ancillary ASIC's required.
  - One set of discriminator threshold per readout chip (does not need trim bits in every pixel cell).
  - Simple, fast programming.

Summary

- The Fermilab effort to develop hybrid silicon pixel detectors started in 1997 and is ~95% complete.
- Allowing this effort to finish successfully will result in the production of state-of-the-art detectors that are likely to be used in a variety of experiments. It will also put Fermilab in a better position to start other vertex detector R&D projects.